Development of a 1U new space camera for EMCCD and CCD sensors with enhanced low-light sensitivity

Olivier Daigle[a], Oleg Djazovski[b], Jean Dupuis[b], René Doyon[c], Farbod Jahandar[c], Sarah Bouguéroua[a], Marie-Eve Ducharme[a], Adam Gilbert[a], Jeremy Turcotte[a], and Yoann Gosselin[a]

[a]Nüvü Camēras Inc., 603-355 rue Peel, Montréal, Qc, Canada, H3C 2G9
[b]Canadian Space Agency, 6767 route de l'Aéroport, St-Hubert, QC, J3Y 8Y9, Canada
[c]Institute for Research on Exoplanets, Département de physique, Université de Montréal, C.P. 6128 Succ. Centre-Ville, Montréal, QC, Canada, H3C 3J7

ABSTRACT

With recent advances in large-scale space telescope missions, new sensors and technologies are made available for use in space for the first time. With the recent developments for the Coronagraph Instrument (CGI) instrument of the Nancy Grace Roman Space Telescope (NGRST), Electron Multiplying CCD (EMCCD) readout electronics and sensors are being qualified for extended use in space. To make this new remote sensing technology available for a wider range of missions, a new space camera version has been developed, with the first units outfitted with the Teledyne-e2v CCD201-20 EMCCD sensor. This novel camera, equipped with proprietary Camera Proximity Electronics (CPE), is built with a balance of space-qualified components and Commercial Off The Shelf components with flight heritage to optimize cost, performance, and reliability. In addition to direct imaging and characterization of exoplanets, the sensitivity of this camera is also enabling Space Situational Awareness applications. The first imaging, random vibration and TVAC testing results of this new 1U camera platform named nüSpace will be presented.

Keywords: EMCCD, Nancy Grace Roman Telescope, CGI, Coronograph, Exoplanet, Photon Counting imaging, Wavefront sensing, Low light camera

1. INTRODUCTION

From the first EMCCD Read-out Electronics (ROE) developed by Nüvü,[1] efforts were put to develop a space qualified version that could deliver an imaging performance comparable to the commercial one. Work made with the Canadian Space Agency (CSA) led to a design whose performance was demonstrated in a relevant environment,[2] and which flew on a stratospheric balloon in 2018.[3] Following those milestones, a smaller, lighter and lower power version of the ROE, the CPE, was developed, qualified and delivered by a Nüvü-ABB team to the Jet Propulsion Laboratory (JPL)[4] to be used as the Direct Imaging (DI) and Low Order Wavefront Sensor (LOWFS) cameras of the CGI instrument,[5] which will fly on the NGRST in 2027.

Although it met the stringent requirements of the CGI, the CPE is a custom made product that is not intended to be directly used on other space missions as the mechanical, thermal and electrical interfaces were matched to the very particular requirements of the CGI. In order to bring this kind of technology to other, more numerous, and also cheaper missions, a new version had to be designed. Starting from the improvements made to the ROE of the CGI, a new design effort was put on making it compatible with CubeSats.[6]

Following the CubeSats standard, a new space CPE, which could fit into a 1U unit of a larger spacecraft, was designed using IEEE parts that are either space qualified or have heritage in space or in a radiative environment. This last option allowed the design to incorporate electronic components that are of a newer technology, which often mean smaller, lower power and higher performance. For instance, the work made on the large particle accelerators over the last decade provided an abundance of literature on the behaviour of several high performance components in a harsh radiative environment.

This paper presents the system requirements of the new space CPE (Section 2), the design of the CPE (Section 3), the results of the laboratory characterization (Section 4), and the results of Thermal Vacuum Chamber (TVAC) and vibrations qualification (Section 5).

Further author information: E-mail: odaigle@nuvucameras.com, Telephone: +1 514 733 8666

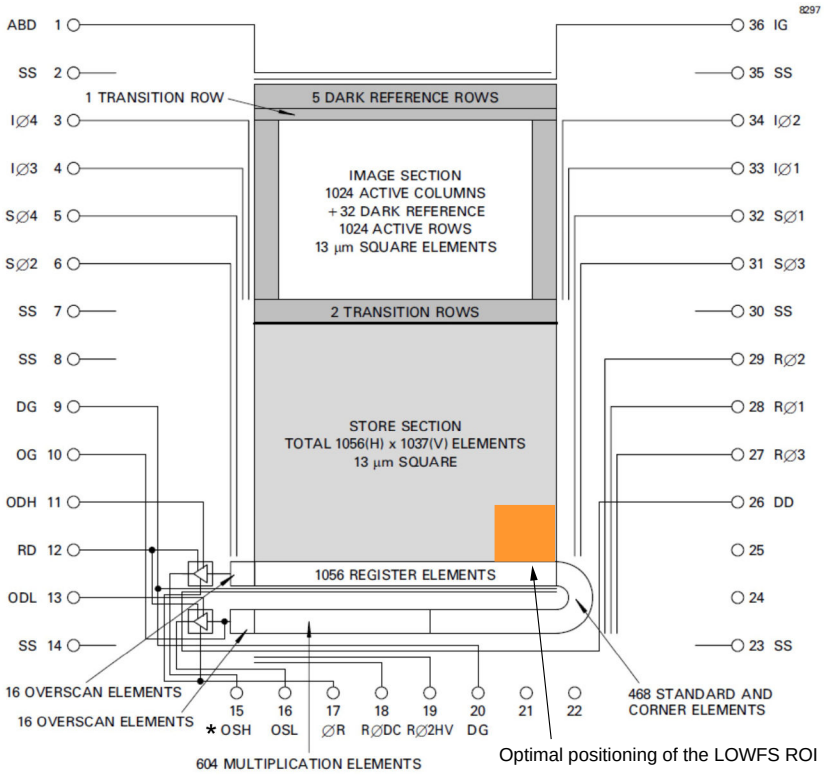

Figure 1: EMCCD device architecture with the LOWFS ROI through the EM amplifier. The device used for LOWFS operation does not have a store shield deposited on the storage section.

2. SYSTEM REQUIREMENTS

In order to be easily integrated in a variety of space missions, the CubeSat standard was adopted, defining a 1U unit as the envelope of the system. For those small satellites, where the power and mass budgets are scarce, the following requirement were adopted:

1. Mass: $\leq$3 kg
2. Volume: $\leq$10 cm $\times$ 10 cm $\times$ 10 cm (1U), including the detector headboard and interface to a passive cooling unit (radiator)
3. Power consumption: $\leq$15 W at 1 FPS

The system was developed to allow imaging with the full active area of the CCD201-20 EMCCD from Teledyne-ev2, a mode referred to as DI, and also with a small sub-region of the sensor in order to allow very fast imaging, a mode referred to as LOWFS. This later mode was developed for the needs of the CGI, where a 50x50 sub-section of the EMCCD is read at a high frame rate (Figure 1), and it requires a version of the CCD201-20 that does not have a store shield[7] to reach the highest frame rate. The requirements for both operational modes are presented in Tables 1, and 2, respectively. Those requirements are driven by the use of an EMCCD as the imaging device, and the required frame rates are to be achieved with a 10 MHz read-out rate, which is the nominal pixel frequency of the system. Those requirements do not restrict the system to be used only with EMCCDs. Standard Charge Coupled Devices (CCDs) could also be read-out with the system, at a different pixel rate and with different noise figures.

In order to meet those requirements, the system was designed to provide the following:

- Generation of 8 Low Voltage low speed triangular clocks (to be used for vertical clocks);

Table 1: Direct imaging PEC.

Parameter	Type	Value
Resolution	Spatial	1024×1024
	Temporal	≥8 fps
	Digital	≥16 bits
Noise	Read-out	<100 e^- (Unity EM gain)
	Thermal	<0.001 e^-/pix/s (1000x EM gain)
	CIC	<0.01 e^-/pix (1000x EM gain)
Well depth	Vertical	>20 ke^-
	Horizontal	>100 ke^-
Bandwidth	Spectral	400–850 nm >50% average and peak of 90%

Table 2: LOWFS PEC.

Parameter	Type	Value
Resolution	Spatial	50×50
	Temporal	≥1300 fps
	Digital	≥16 bits
Noise	Read-out	<100 e^- (Unity EM gain)
	Thermal	<0.1 e^-/pix/s (1000x EM gain)
	CIC	<0.1 e^-/pix (1000x EM gain)
Well depth	Vertical	>60 ke^-
	Horizontal	>100 ke^-
Bandwidth	Spectral	400–850 nm >50% average and peak of 90%

- Generation of 6 Low Voltage high speed clocks (to be used for horizontal clocks);
- Generation of 2 High Voltage clock (up to 50 Volts) with a frequency of 10 MHz (to be used for the EM gain process);
- Digitization of up to four video outputs (simultaneously or not) to accommodate both the EM and Conventional outputs of the EMCCD and multi-channel CCDs. The digitization is performed at 16 bits, 100 MHz with a digital CDS implemented in VHSIC Hardware Description Language (VHDL);
- 10 DC levels with the possibility to adjust them (for bias generation);
- A Camera Link (CL) interface for communication of the pixel data to a host and an input for commands that can also run in modified Channel Link mode (3 data pairs instead of 4).

The system is ought to be used mainly in Low Earth Orbit (LEO), which drove the environmental requirements presented in Table 3. This does not, however, restrict the system to be used in other orbits and even out of the Earth's gravitational influence. More specific modelling would be required in those cases.

3. DESIGN

The system is designed around a stack of 5 Printed Circuit Boards (PCBs) (Figure 2), having the following functions:

1. A power supply board, which takes the spacecraft bus power and converts it into the required secondary voltages;
2. A digital board, which houses the digital core of the electronic controller;
3. A vertical drive board, which generates the low speed signals required by the vertical clocking of the CCD;

Table 3: Environmental requirements.

Parameter	Value
Orbit	Low Earth Orbit
Environment	Vacuum
Random vibrations	6.8 g RMS at 1 minute/axis 20-2000Hz
Cooling	Passive cooling system
CPE non-operational temperature range	-40 to +60°C
CPE operational temperature range	-35 to +60°C
EMCCD non-operational temperature range	-150 to 125°C
EMCCD operational temperature range	-135 to +60°C
EMCCD performance temperature range	-110 to -85°C
EMCCD performance temperature stability	$\pm$0.1°C
SEL LET_{TH}	$>$62.5 MeV·cm^2/mg
TID	$>$15 krad

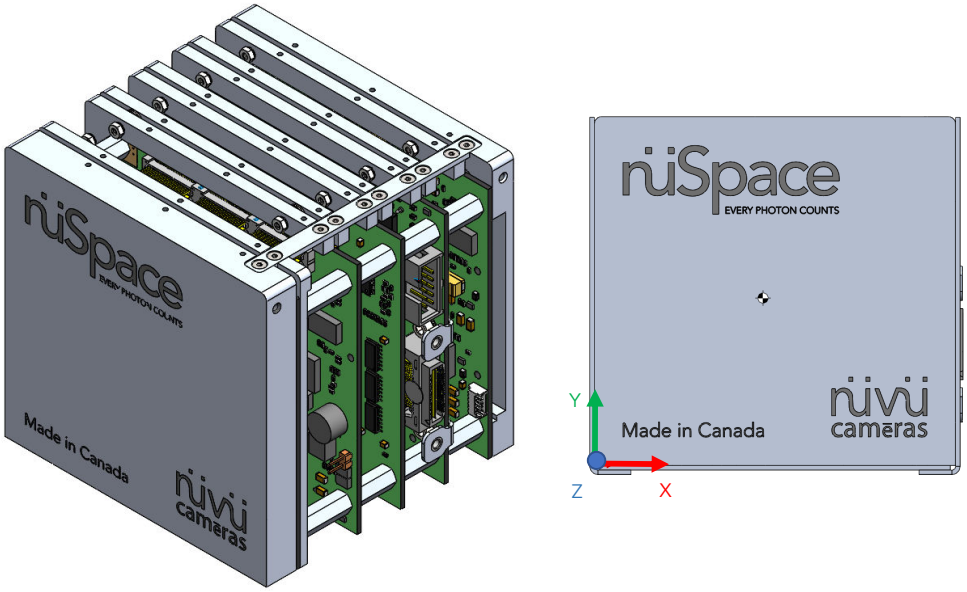

Figure 2: Overview of the prototype and its coordinate system

4. A horizontal drive board, which generates the high speed signals required by the horizontal clocking of the CCD as well as digitizing the video outputs;
5. A headboard, which holds the EMCCD.

3.1 Electronic design

The electronics of the CPE can be split into four high-level components:

- The power supply;
- The digital core, which implements the sequencer, the digital interface of the pixel data, and the house keeping processor;
- The analog core, which implements the EMCCD's clocks generation and shaping, generation of DC levels, video signal conditioning and digitization;
- A telemetry system, which measures and monitors the CPE.

Table 4: Overview of the RT PolarFire.

Parameter	Value[8]
Part number	RTPF500T[a]
Lithography	28 nm
Logic elements (4LUT + DFF)	481 k
Math blocks (18x18 MACC)	1480
LSRAM Blocks (20 kbits)	1520
μSRAM Blocks (64x12 bits)	4440
Total RAM (Mbits)	33
μPROM (kbits)	513
User PLL	8
Total user Input-Outputs (I/Os)	584
SEU mitigation	SRAM SECDED
Configuration SEU	Immune up to 80MeV·cm^2/mg
SEL LET$_{TH}$ (MeV·cm^2/mg)	>82.1 (1.8 V I/Os) 68.5 (2.5 V I/Os)[9] 48 (3.465 V I/Os)[10]
TID (krad)	100[b]
Temperature range	-55°C – 125°C
Package	1509 CCGA
Flow	Up to QMLV

[a] As per Microchip information, it uses the same die as the commercial MPF500T. Only the qualification flow varies.
[b] Total ionizing dose test reports available for each wafer lot.

3.1.1 Power supply

From a single 16–26 V from the spacecraft, the power supply module generates the required secondary voltages to operate the CPE. Those secondary voltages are generated with Switched Mode Power Supplies (SMPS) that are synchronized to the read-out by the Field Programmable Gate Array (FPGA). This allows for the residual of the switching artifacts to be fixed within the images generated, which can then be subtracted with bias frames.

The secondary voltages that drive digital Integrated Circuits (ICs) are current-monitored to detect latch-ups that could occur. A fault protection mechanism scan those current measurements and allows for shutting down the CPE if a potentially destructive latch-up would occur.

The power supply module is also used to generate an adjustable 0–15 V output that can be used to power a heater to close a control loop for the EMCCD temperature control.

3.1.2 Digital core

The design of this component is an evolution of the NGRST design, with the main difference being in the FPGA implementing the digital core. Whilst the NGRST design employed a Virtex5-QV from Xilinx, this new design uses the Radiation Tolerant (RT) PolarFire from Microchip. The resources made available by this FPGA as well as its radiation performance are outlined in Table 4.

Soft processor The digital core implements a RISC-V soft processor to handle configuration, command and control and house-keeping tasks. The command and control data are received by the soft processor through a Universal Asynchronous Receiver-Transmitter (UART) port using a custom communication protocol. The C code of the soft processor interacts with the custom VHDL components that handle all of the real-time tasks of the CPE. The soft processor is also responsible for scrubbing operations on the volatile and non-volatile memories.

SEE mitigation Just like the well-known RTG4, the PolarFire is a flash-based FPGA, and its configuration memory immune to Single Event Upset (SEU) up to 80MeV·cm^2/mg.[8] The configuration memory immunity makes it possible to avoid using a configuration scrubber, with all of the complexities it imposes when an error is detected. When using $\leq$2.5 V I/Os, the SEL LET$_{TH}$ is 68.5MeV·cm^2/mg.[10] For this reason, the design does not employ 3.3 V I/Os.

The PolarFire provides support for a TMR-ed design as well as spatial placement within the FPGA. The tool chain provides an attribute "syn_radhardlevel" which is used for implementing the registers functions as single native D-type Flip-Flop (DFF)/register cells or Triple Modular Redundancy (TMR) registers. In this case, each register function that is implemented with the TMR consumes three registers and one Look-up Table (LUT). The "syn_radhardlevel" attribute is supported at Global, Module Instance, and Register View levels in the Register Transfer Level (RTL) or FPGA Design Constraint (FDC). The TMR attribute can be applied Globally, to an instance or to a register.

Test data shows that when the three registers that comprise a TMR triplet are physically spaced apart from each other on the die, this improves (lowers) the SEU rate of the TMR register function.[11, 12]

When "syn_radhardlevel" TMR is specified globally, registers associated with memory and multipliers are packed inside Random-access memory (RAM) and Digital Signal Processor (DSP) blocks, and are not triplicated. Also, the "syn_radhardlevel" TMR attribute triplicates the inferred Sequential Logic Element (SLE) register instance only. SLE latch instances are not triplicated by this attribute. The SLEs should be inferred by tool "SynplifyPro", the synthesis tool.

The PolarFire provides the capability of having Error Correction Code (ECC) on the Large SRAM (LSRAM).[13] The LSRAM have built in Single Error Correction, Double Error Detection (SECDED) and interleaving to prevent multi-bit upsets. The memory provides two signals that would indicate the nature of the error: single-bit error detection (correction) and a double-bit error detection. In case of single bit errors, the data is corrected upon reading it and therefore scrubbing is implemented on the embedded side. The double bits are only detected and not corrected. In that case further protective measures are implemented. For the context, the LSRAM are used as the runtime memory of the soft processor.

The micro SRAM (μSRAM), used for buffers and First-In, First-Out (FIFO) or RTL inferred memories are not ECC protected by design. Therefore, there is a need to implement the logic to read and correct those as well. A Reed-Solomon algorithm is implemented as it allows 32 bits words to be corrected with 8 bits of parity. Up to 1 bit of error per 4 bits nibbles of the 32 bits can be corrected, and two bits errors are detected.

In the case of realtime memories where error detection and correction could not be interleaved with the access, the memories are duplicated so that one set is scrubbed/corrected while the other is in use. In this architecture, one memory device is actively used whilst the other is being read sequentially to check for data corruption through a custom implementation of ECC. Upon detecting a correctable error the core writes back that memory location the corrected data. After having swept the whole memory array, the active and scrubbed memory devices are swapped, which allows for the scrubbing of the device that was previously used while the one that was being scrubbed is now used actively. When writing to the memory, the scrubbing has to be interrupted so that both memory devices are written to. This duplication is transparent to the modules that use the memory, from their perspective data is available when required in sequential order or at random. Uncorrectable errors are reported so that actions can be taken at a higher level to prevent its use.

The CPE implements a flash memory to hold configuration data used to sequence the read-out of the EMCCD and the Embedded Software (E-SW) system image. The flash's data is duplicated within the device, scrubbed and CRC-ed to check for errors. If a block of the memory is found to be corrupted, a copy of it can be fetched so that operations can go uninterrupted. If both the main and the backup copy of a block of the flash are corrupted, this condition is detected and the configuration is flagged as invalid. This allows a certain level of redundancy, and it insures a corrupted configuration can't be loaded into the CPE.

3.1.3 Analog core

The CPE generates all of the required DC biases and clock signals to drive the EMCCD as listed in Table 5, and synchronizes the Analog to Digital Converter (ADC). All clocks have low and high levels that are independently adjustable within the depicted range.

All of the analog clocks are synchronized by digital signals generated by the FPGA's sequencer. Those signals dictate the state of the clock (low or high), and the analog part of the clock generation handles the shaping of the clock to the designed shape (triangular or RC), within the low and high levels set. The flexibility in the generation of the clocking schemes

Table 5: Signals generated by the CPE's analog core.

Signal name	Signal type	Timing resolution	Rise/fall time	Range
$S\phi_{1\text{-}4}$	Triangular clock	1.25 ns	30 V/μs	-7 V – 14 V
$I\phi_{1\text{-}4}$	Triangular clock	1.25 ns	30 V/μs	-7 V – 14 V
$R\phi_{1\text{-}3}$	RC clock	1.25 ns	20 ns	-7 V – 14 V
DG	RC clock	1.25 ns	20 ns	-7 V – 14 V
ϕR_{LH}	RC clock	1.25 ns	10 ns	-7 V – 14 V
$R\phi_{2HV}$	LC resonant clock	1.25 ns	Sinusoid at 10 MHz	-1.8 V – 61.8 V[a]
Biases	DC	–	–	-5 V – 30 V[b]

[a] Software-limited to 50 V (configurable) to prevent exceeding the EMCCD absolute maximum rating.

[b] Depending on the bias. The range is adapted individually to the EMCCD typical range and absolute maximum rating.

offered by the CPE design is of importance as this is what allows it to support, within the same hardware configuration, the different operational modes, from the >1k fps imposed by the LOWFS mode to the lower frame rate of the DI mode.

Video signal conditioning is made with a chain of high speed, low noise amplifiers to bandwidth-limit, scale and convert the single-ended video signal into differential. This signal is then fed to a 100 MSPS 16-bits ADC which is constantly sampling. At a pixel rate of 10 MHz, 10 samples per pixel are generated and those are processed in a Digital Correlated Double Sampling (DCDS) implemented in VHDL.

3.1.4 Telemetry system

The CPE implements a telemetry system to gather data about the status and the health of the system, such as current, voltages, temperatures and scrubbing data. The data measured by the telemetry system can also be used internally to implement fault protection and run digital proportional–integral–derivative (PID) loops for temperature control. The telemetry is gathered by the soft-core processor through low speed ADCs and digital inputs, with some other data coming from the custom VHDL components of the digital core or the FPGA itself. The telemetry data is transmitted to the spacecraft upon request by it, through the command interface.

3.2 Mechanical and thermal design

The CPE is compatible with the footprint of the PC-104 PCBs standard that is widely adopted by CubeSats.[14] The five PCBs of the CPE are stacked within the height of a 1U unit, and the detector's headboard sits on top of the stack to allow the optical payload to be placed higher up in the spacecraft.

Except for the headboard, each one of the PCB has a thermal interface to the structure of the CPE, which allow the dissipation of the heat they generate. Although the overall power consumption of the CPE is low (see Section 5.1.4), the power dissipation is not evenly split across the PCBs and the choice was made to thermally sink all of them to keep their temperature uniform. The thermal interface of those PCBs is made to be tied to a radiator on the spacecraft. Thermal modelling has shown that a single 10 cm $\times$ 10 cm surface allowed to dissipate the heat generated by the CPE and keep it within its operating range for most orbits. However, the specifics of each mission have to be taken into account to figure the right dissipation scheme. The thermal interface of the CPE can be adapted to suit particular needs.

The headboard holding the EMCCD is thermally decoupled from the CPE to allow the EMCCD to be cooled to its performance temperature range. The EMCCD is attached to a thermal strap connected to an independent radiator. A surface of 20 cm $\times$ 10 cm is required to sink the heat dissipated by the EMCCD and stray heat carried through the copper traces of the headboard, and maintain a temperature in the intended range. Redundant PT100 temperature sensors are used for monitoring the temperature of the EMCCD, and a resistive heater allows for closing an active control loop.

4. IMAGING PERFORMANCE TESTS

The imaging performance tests were performed with the CPE interfaced to a Nüvü Liquid Nitrogen (LN_2) cryostat (the Nüvü's EMN2) containing a CCD201-20 EMCCD. For that purpose, a special interface card has been designed to allow the CPE to be connected to the EMN2's hermetic connector through its headboard interface. The EMN2's controller box was also modified to allow the CPE to fit in (Figure 3). The EMCCD was stabilized at -85°C.

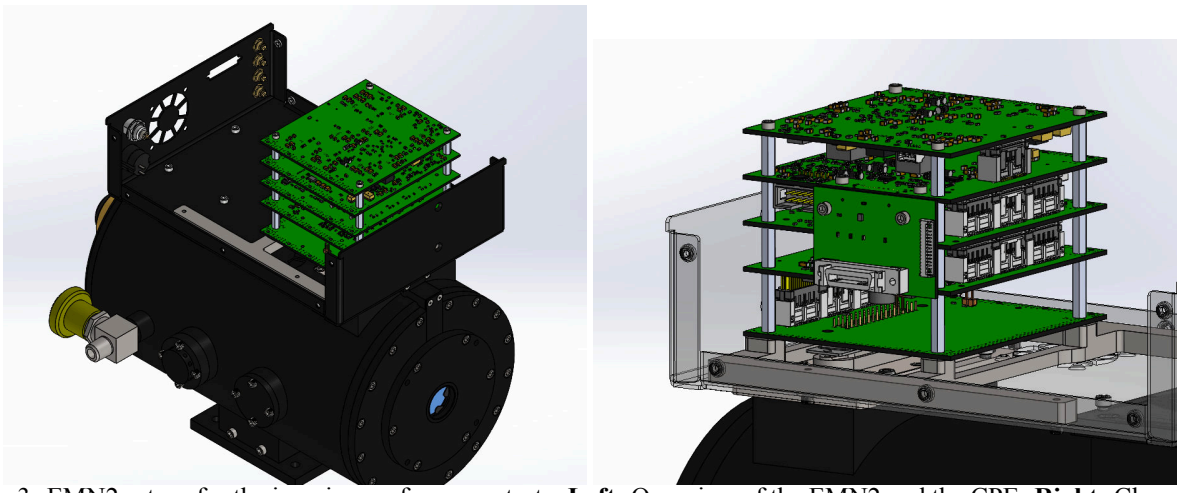

Figure 3: EMN2 set-up for the imaging performance tests. **Left**: Overview of the EMN2 and the CPE. **Right**: Close-up of the CPE, the EMN2 interface card and the CameraLink interface card.

Since the EMCCD is held within the EMN2 enclosure, the tests can be performed in a lab environment. A CameraLink adapter board was designed to allow for the CPE to be plugged into a commercial CameraLink frame grabber, which means that the CPE could be controlled through Nüvü's software suite.

For both the DI and LOWFS modes, tests consisted of acquiring Photon Transfer Curves (PTCs)[15] to measure Read-out Noise (RON), Vertical Full Well (VFW), Horizontal Full Well (HFW), and linearity (Sections 4.1.1 and 4.1.2). Dark frames were acquired at high Electron Multiplying (EM) gain to measure the dark current and Clock Induced Charges (CIC) (Sections 4.2.1 and 4.2.2). Finally, images were acquired at the maximum frame rate to confirm the capability of the CPE to operate at the required refresh rate (Sections 4.3.1 and 4.3.2).

4.1 RON, VFW and HFW measurements through the EM amplifier at 10 MHz at unity gain

4.1.1 Direct Imaging mode

The RON of both CPEs was measured with the PTC method, and by using increasing exposure time to generate a variation of the signal as seen by the EMCCD.

The data (Figure 4) show that the system's response is $\sim$12.2 e^-/ADU, and the read-out noise is $\sim$60 e^-, which means that the standard deviation of a bias image is 4.9 ADU. The acquisition was made with a vertical clocking frequency of 800 kHz, up to a VFW of $\sim$35 ke^- with a linearity within the $\pm$1% range. The linearity at low flux is always a challenge to measure, which explains the scattering of the data points for fluxes $<$1 ke^-.

The HFW was measured by taking a PTC and using a vertical binning of 8 to increase the signal level in the horizontal register. In this way, the horizontal register saturated at 202.7 ke^-.

4.1.2 Low Order Wavefront Sensor mode

Similarly, PTCs were acquired in LOWFS mode (Figure 5). Although it is not expected to change drastically from what was measured in Section 4.1.1, the data shows that the system's response is $\sim$13.9 e^-/ADU, and the read-out noise is $\sim$66 e^-, which means that the standard deviation of a bias image is 4.8 ADU. The acquisition was made with a vertical clocking frequency of 800 kHz, up to a pixel well of $\sim$75 ke^- with a linearity within the $\pm$1% range. The HFW measurement showed a saturation of the horizontal register at 133.3 ke^-.

4.2 Dark current and CIC measurements

4.2.1 Direct Imaging mode

In order to disentangle the horizontal and vertical CIC components, the EMCCD is over-scanned in both the vertical and horizontal directions as in [4].

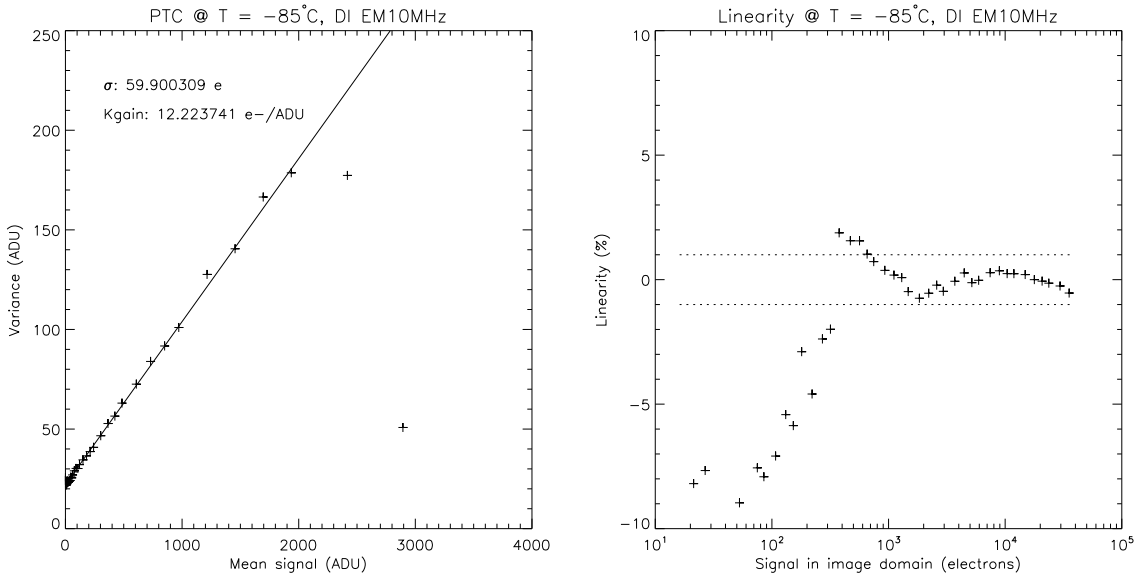

Figure 4: PTC results in DI mode. **Left**: Photon Transfer Curve. **Right**: Linearity. The dotted lines show the $\pm 1\%$ boundaries.

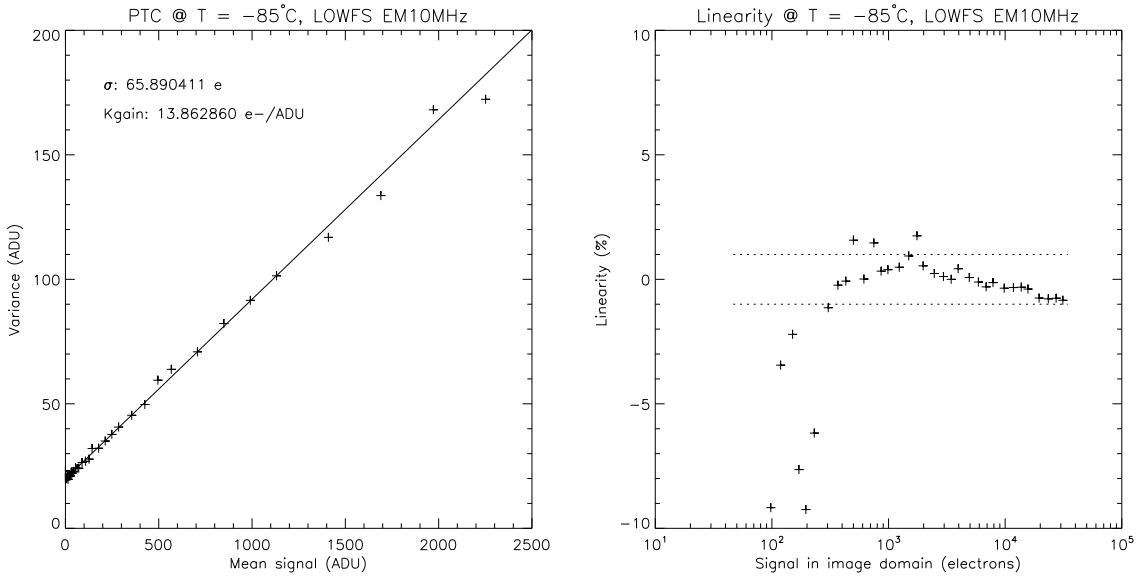

Figure 5: PTC results in LOWFS mode. **Left**: Photon Transfer Curve. **Right**: Linearity. The dotted lines show the $\pm 1\%$ boundaries.

Table 6: CIC Measurements at −85°C. **Top**: DI mode. **Top**: LOWFS mode

EM gain	Background (e^-/pix/im)	H CIC (e^-/pix/im)	V CIC (e^-/pix/im)
1000	0.00120	0.00076	0.00051

EM gain	Background (e^-/pix/im)
1000	0.00142

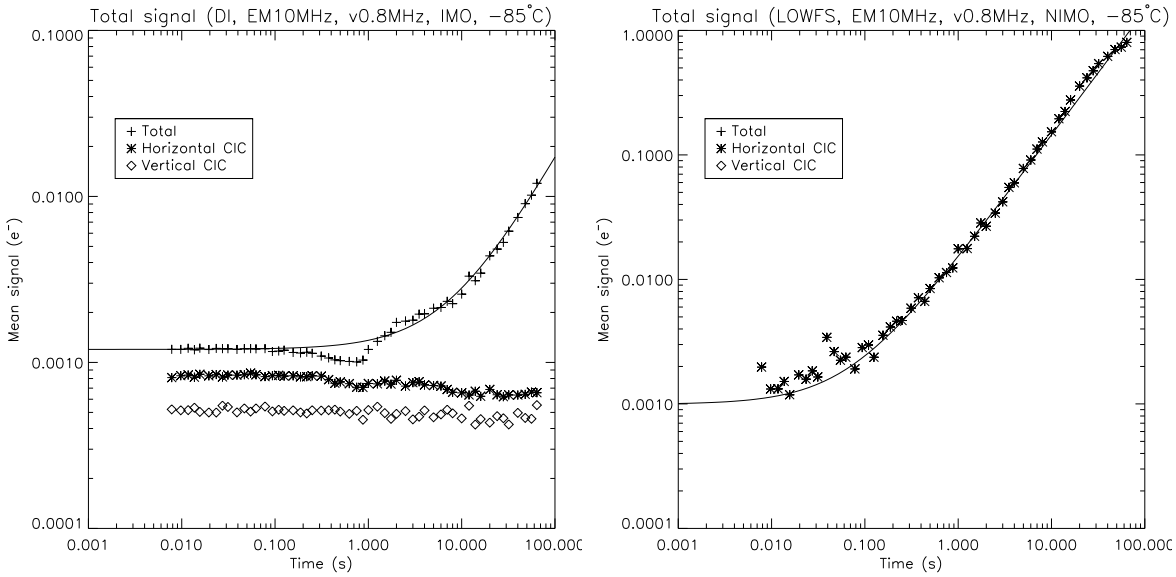

Figure 6: Total Background Signal Measured in PC at −85°C and at an EM Gain of 1000. The values are corrected for the events loss due to the PC threshold. **Left**: DI mode. **Right**: LOWFS mode.

The total background signal is measured with a 0-s effective exposure time. Thus, the total background signal measurement includes the dark current generated during the read-out process as well as the CIC. The measurement errors are within ±0.0002 e^-/pixel/im which explains the discrepancy between the total background signal measured and the sum of the horizontal and vertical CIC. The vertical frequency used is 800 kHz, which is the maximum vertical frequency the CPE can drive the CCD201-20 without going beyond its derated maximum output current for the vertical clock drivers. The measurements are made with a 5σ threshold to reflect the Photon Counting operation.

The dark current measurements are performed at an EM gain of 1000. The dark current is measured by fitting a slope to the signal acquired by the camera for exposures from 0 to 64 seconds.

The CIC results are presented in Table 6. At −85°C, the dark current measured is 0.00016 e^-/pixel/second.

Figure 6 shows an example of the data acquired to measure both the background signal, the horizontal and vertical CIC, as well as the dark current.

4.2.2 Low Order Wavefront Sensor mode

Because of the specific nature of the 50 × 50 pixels Region of Interest (ROI) in the LOWFS mode, it is not possible to do horizontal overscan. This implies that it is not possible to measure the contribution of the horizontal and vertical components of the CIC to the total background level. The CIC results are presented in Table 6.

At −85°C, the dark current measured is 0.013 e^-/pixel/second. This figure is higher than for the DI mode (Section 4.2.1) as the EMCCD is clocked in Non-Inverted Mode Operation (NIMO) for the LOWFS operation in order to facilitate the back-clocking one has to do to quickly clear the ROI of the LOWFS from residual charges accumulated during the integration of the previous frame.

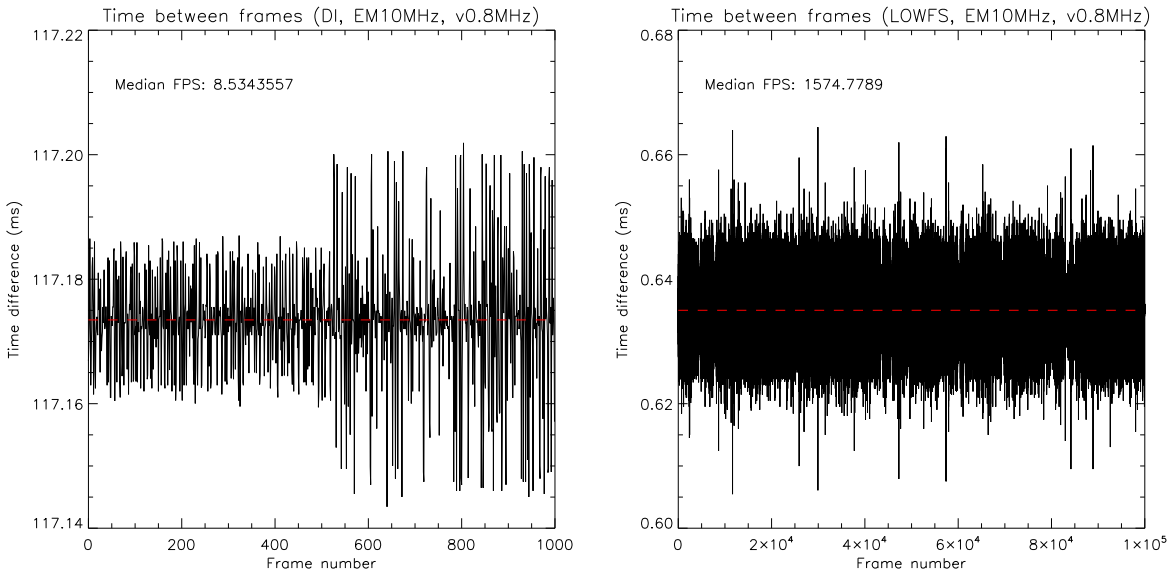

Figure 7: Time difference between the arrival of consecutive frames in DI measured on the acquisition computer. **Left**: DI mode. **Right**: LOWFS mode.

4.3 Maximum Full Frame Refresh Rate

4.3.1 Direct Imaging mode

The measurement of the time difference between the arrival of the 1000 frames are presented in Figure 7. The frames are composed of 1037 lines of 1072 pixels each and are followed by a line of overscan that is used as a dark reference to get the zero point of the image, and lastly a line containing the telemetry data generated by the CPE.

As the time of arrival is measured on the receiving computer, the jitter in the measurement can be seen as the processor can take a variable amount of time to respond to the interrupt for receiving an image. Overall, however, the time difference is very stable. The data shows a median of ∼117.17 ms between frames, which equates to a rate of ∼8.5 FPS.

4.3.2 Low Order Wavefront Sensor mode

The measurement of the time difference between the arrival of 100 000 LOWFS frames are presented in Figure 7. The frames are composed of 50 lines of 52 pixels to accommodate the limitation of the frame grabber to sample images having a width that is divisible by 4.

The data shows a median of ∼0.635 ms between frames, which equates to a rate of ∼1575 FPS. The jitter in the data is due to small differences in the processing time of the images on the host computer rather than jitter in the output of the images from the CPE.

5. QUALIFICATION

5.1 Thermal vacuum campaign

5.1.1 Setup

The CPE underwent TVAC testing at CSA's David Florida Laboratory (DFL) in Ottawa in April 2023. The TVAC Optical Ground Support Equipment (OGSE) was designed to illuminate the EMCCD with a flat field through the internal reflection of a Light Emitting Diode (LED) mounted on the headboard whose luminosity was adjustable. Since only one thermal control loop was available in the TVAC used, it was decided to thermally link the EMCCD to the CPE. Hence, it was not possible to stabilize the temperature of the EMCCD independently. Although the TVAC campaign was made with a CCD201-20 EMCCD, it was not the same as the one used for the imaging performance tests.

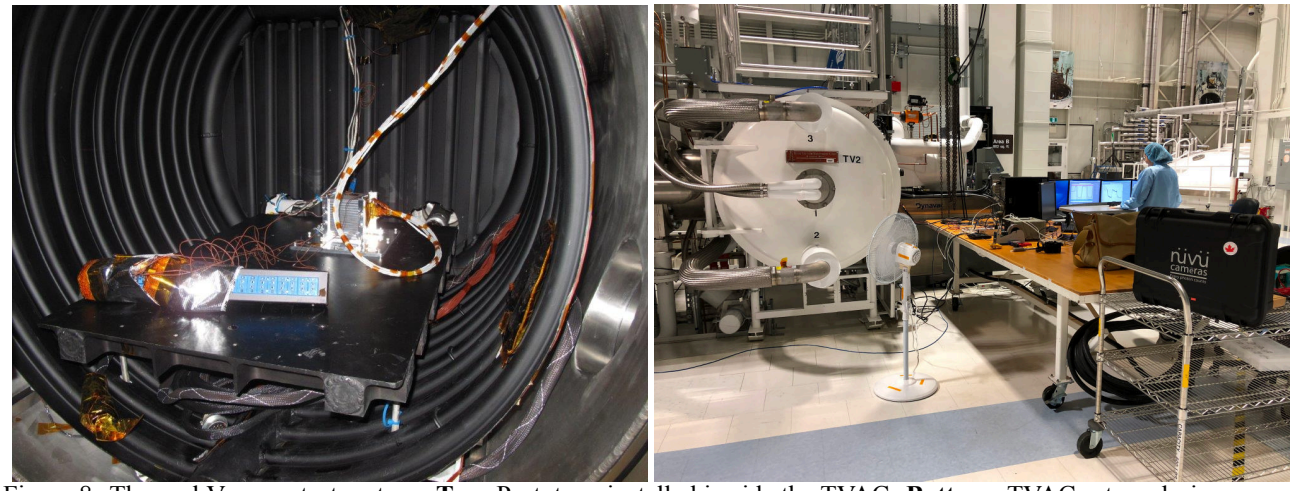

Figure 8: Thermal Vacuum tests set-up. **Top**: Prototype installed in side the TVAC. **Bottom**: TVAC set-up during operations.

Table 7: List of external temperature sensors.

Name	Location	Purpose
`Plate front`	Interface plate, front	Monitors the temperature of the TVAC interface
`Plate back`	Interface plate, front	Monitors the temperature of the TVAC interface
`Front panel`	Prototype, front panel	Monitors the temperature of a face perpendicular to the PCB stack
`Side panel`	Prototype, side panel	Monitors the temperature of a face perpendicular to the PCB stack
`CCD rad`	Prototype, CCD panel	Monitors the temperature of a face close to the CCD

The test set-up is shown in Figure 8. The Figure shows the prototype installed on the TVAC's plate through a mechanical interface. It was then connected, via power cables and Camera Link cables, to a power supply and a computer that sit outside of the TVAC. The computer ran Nüvü software suite allowing for remote control and functional tests. Additionally, several temperature sensors were placed on both the TVAC and prototype and were connected to a read-out circuit (Table 7, Figure 9). Moreover, the prototype's integrated temperature sensors were read-out throughout the TVAC campaign. Those are enumerated in Table 8.

Thermal vacuum tests procedure was derived from NASA's standards for qualification.[16] The test profile summarizing the executed test parameters are presented in Figure 10 and Table 9. All tests were executed at a pressure of 10^{-4} Torr or lower.

Table 8: List of internal temperature sensors.

Name	Location	Type	Purpose
`Enclosure`	Prototype enclosure	Thermistor	Monitors the temperature of the housing of the prototype
`Power`	Power supply board	Thermistor	Monitors the temperature of the power supply board
`ADC0`	Digital board	Internal to ADC	Monitors the temperature of the digital board
`Vert`	Vertical drive board	Thermistor	Monitors the temperature of the vertical drive board
`ADC1`	Vertical drive board	Internal to ADC	Monitors the temperature of the vertical drive board
`Horiz`	Horizontal drive board	Thermistor	Monitors the temperature of the horizontal drive board
`RTD0`	CCD cold finger	PT100	Monitors the temperature of the CCD
`RTD1`	CCD cold finger	PT100	Monitors the temperature of the CCD
`FPGA`	FPGA die	Internal to FPGA	Monitors the temperature of the FPGA die

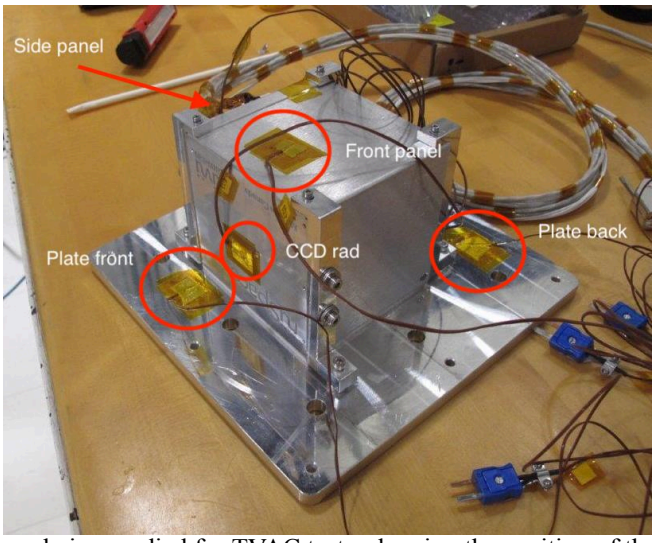

Figure 9: Picture of the prototype being readied for TVAC tests, showing the position of the external temperature sensors.

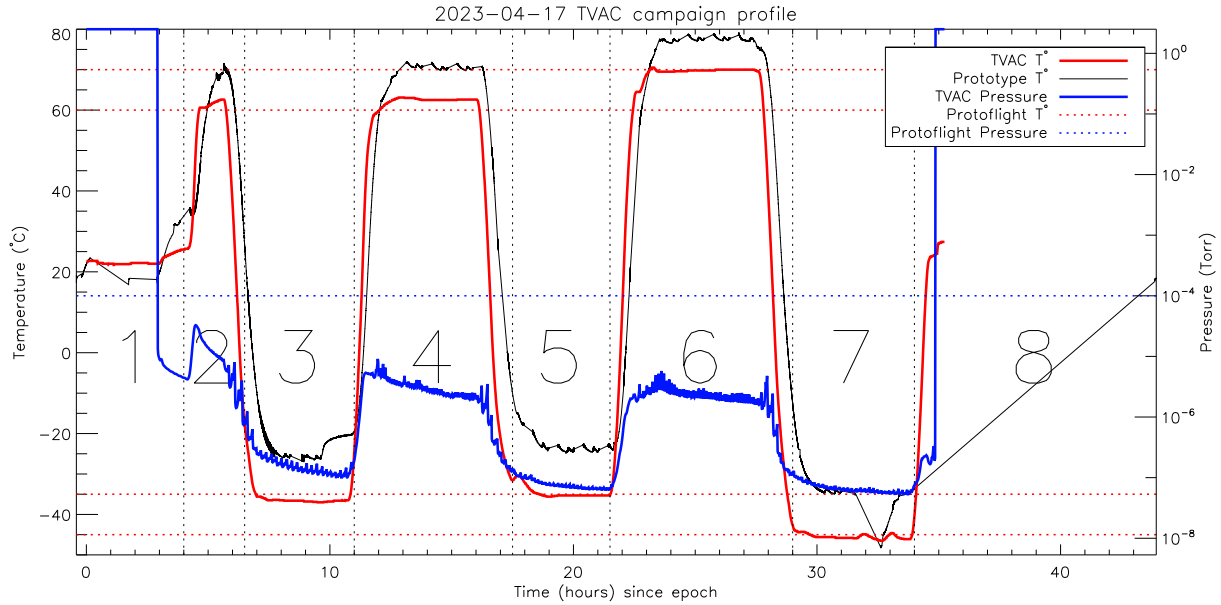

Figure 10: Thermal cycling profile as executed during the TVAC campaign. The horizontal black dotted lines shows the 70, 60, −35, and −45°C temperature plateaus for the operational and protoflight requirements. The horizontal blue dotted line delimitates the maximum TVAC pressure requirement. The vertical dotted lines delimit the plateaus exerted. They are numbered from 1 to 8 for later references.

Table 9: List of TVAC tests objectives, as executed.

Cycle	Plateau(s)	Description	Temperature range	Soak time	Pressure
1	1	Installation Operability at low pressure Reduced functional tests	Ambiant (∼22°C)	∼1 hour	$< 10^{-4}$ Torr
2	2, 3	Initial verification of operability in vacuum and verification of operational temperatures of the controller. Functional tests	−35±3°C – +60±3°C	>1 hour	$< 10^{-4}$ Torr
3	4, 5	Operability in vacuum and verification of operational temperatures of the controller. Functional tests	−35±3°C – +60±3°C	4 hours	$< 10^{-4}$ Torr
4	6, 7	Operability in vacuum at Protoflight temperature range. Functional tests Cold and warm boot tests	−45±3°C – +70±3°C	4 hours	$< 10^{-4}$ Torr
5	8	End of campaign Operability at ambiant pressure Reduced functional tests	Ambiant (∼22°C)	<1 hour	Ambiant pressure

The temperature range was defined by the minimum and maximum expected temperature with margins from each extreme of 10°C. For this project, based on the preliminary thermal simulations, the minimum temperature expected was set −35°C and the maximum was set to +60°C. Therefore, the thermal vacuum test temperatures extremes were set to −45°C and +70°C with a tolerance of ±3°C.[17] Temperature changes were followed by a stabilization time.[18] This reference temperature was measured at the interface plate between the prototype and the TVAC plate. The time at plateau temperatures (hot or cold) were defined to be 4 hours after the first cycle. At each plateau, functional tests were performed. The results of those tests are presented in Sections 5.1.3.

5.1.2 TVAC measured temperature profiles

Throughout the TVAC campaign, the temperature sensors enumerated in Section 5.1.1 were monitored. The recorded profiles are presented in Figures 11 and 12 for the external, and internal sensors, respectively.

All of the sensors measuring the temperature of the prototype settled to about 10°C warmer than the interface at the plateaus with little differences. This represent the loss due to the thermal resistance of the interface between the plate and the prototype, and shows a very small gradient across the prototype.

The dip in the prototype temperature during plateau #7 shows when the prototype was powered off until it reached the temperature of −45°C. It was then switch back on as a cold boot test. Since the CPE exhibited no power dissipation during the time it was powered off, the cold boot test did happen at the cold protoflight plateau set point of −45°C. The loss of the telemetry information during this plateau is due to the powering off of the CPE for the cold boot test. The cold boot test at −45°C was successful.

A hot boot test was made during plateau #6. After three hours of stability, the CPE was switched off for a period of 30 s before being powered back on. The hot boot test at +70°C was successful.

5.1.3 Functional tests results

The measurements were performed at each of the plateaus identified in Figure 10. The results are standard PTC curves, similar to those presented in Section 4. In TVAC, however, since the temperature of the EMCCD was not stabilized, it varied in the same fashion as the temperature of the CPE, see `RTD0` and `RTD1` curves in Figure 12. Hence, the dark current generated by the EMCCD varied widely between the cold and warm plateaus, and it also varied throughout a PTC

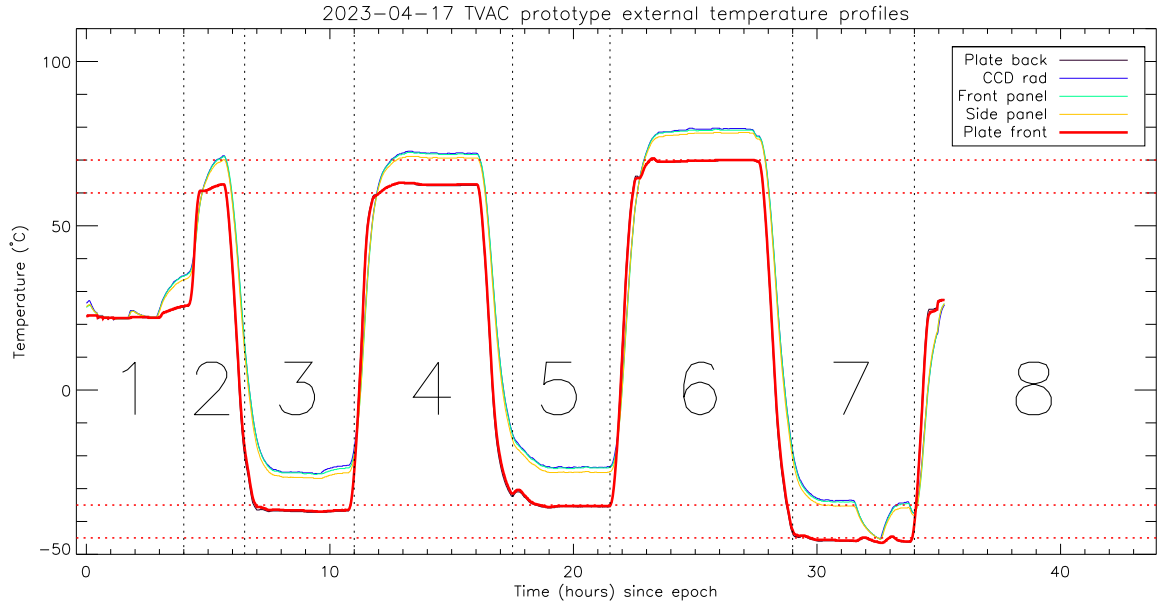

Figure 11: External temperature sensors during TVAC campaign

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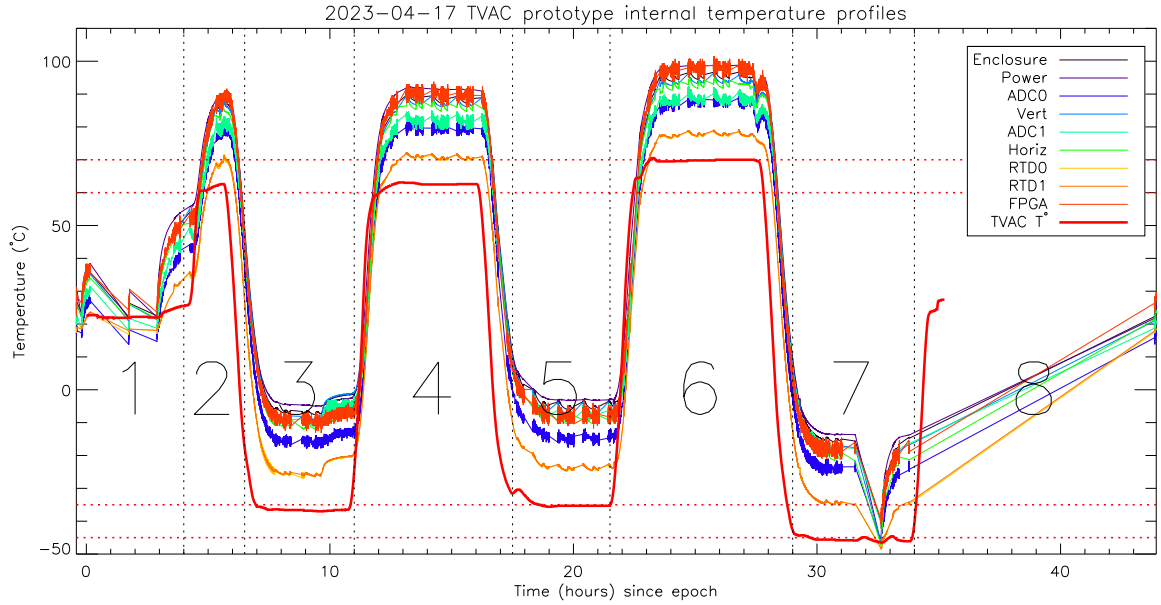

Figure 12: Internal temperature sensors during TVAC campaign. The dip in the measured temperatures at T_0+32.5 h represents the cold boot test.

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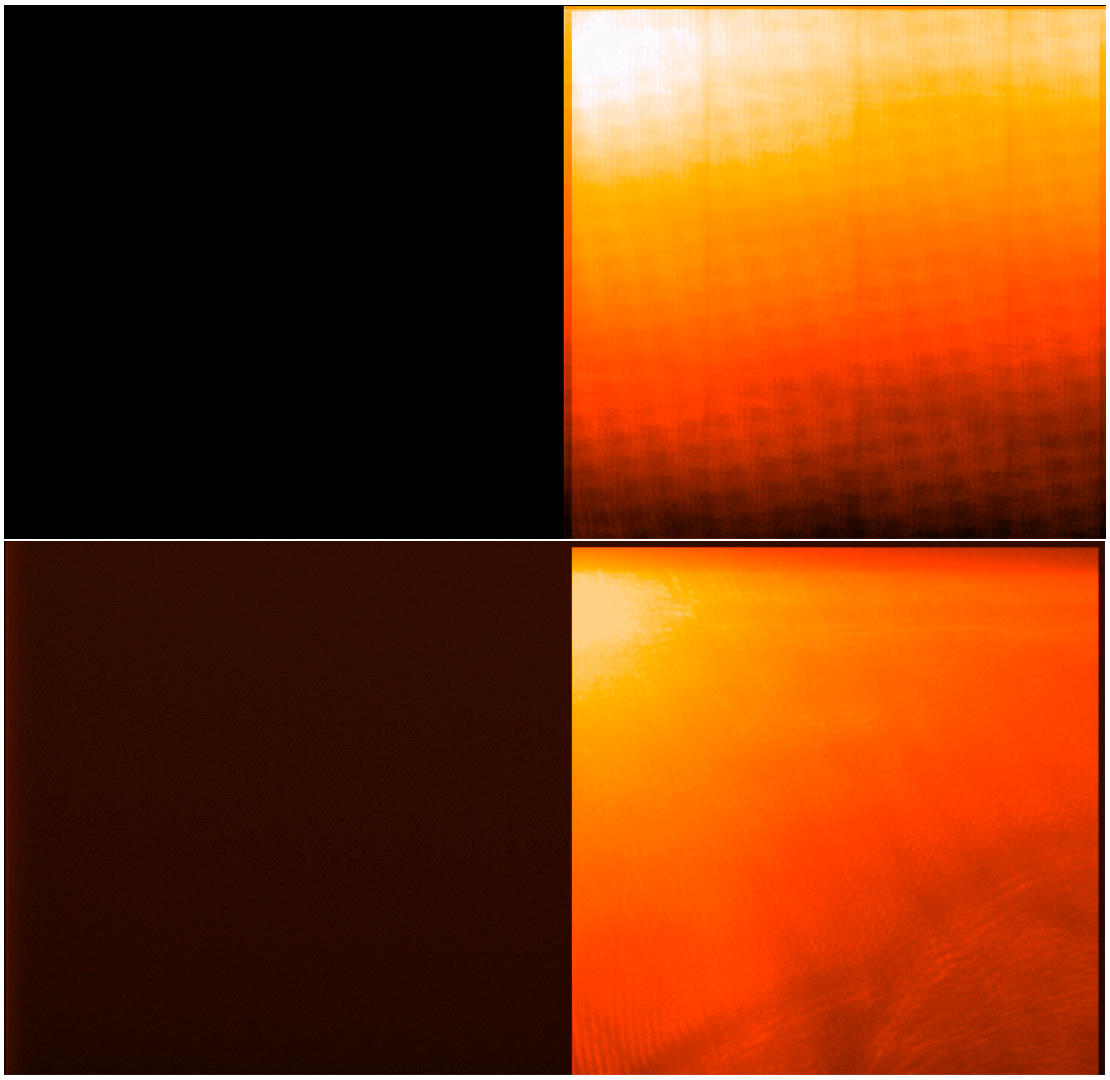

Figure 13: Images captured with the prototype in TVAC, in DI mode. **Top**: During a warm plateau (#4). **Bottom**: During a cold plateau (#5).

acquisition since the temperature of the sensor drifted as a result of the read-out. As a consequence, the linearity measured does not represent the true linearity since the level of signal (photo-electrons and thermally generated electrons) seen by the sensor varied. For this reason, the linearity data is not presented. Example of images taken in DI mode during warm and cold plateaus are shown in Figure 13. They show the image area (on the right) and the overscan region (on the left) that were used as a reference for the RON. For the warm image, the dark current pattern induced by the back-thinning process of the EMCCD is clearly visible.

The PTC results for all of the plateaus are presented in Table 10. The PTC curves for some of the plateaus are presented in Figure 14. In the case of the warm plateau, the PTC overestimates the read-out noise, although the RON in ADU is computed properly. The overestimation of the RON is due to the warm EMCCD that generates a high level of dark current, which renders the capability of taking a dark reference frame impossible. Since the RON is computed from the standard deviation of a dark frame, that computation is biased by the shot noise of the dark current. The values in Table 10 are corrected in that respect. The horizontal overscan region of the image, which is not subjected to the dark current, is taken as a reference for the RON in ADU. The RON in electrons is then computed by multiplying the k-gain by the RON in ADU.

The exact VFW could not be computed for all of the plateaus as the light level set was not high enough. Through the

Table 10: PTC results in TVAC for the DI mode.

Plateau	k-gain	RON (ADU)	RON (e^-)	VFW (e^-)
1	13.01	4.46	58.02	>23.8k[1]
2	<15.21[2]	4.86	<72.91	30k
3	12.65	4.44	56.16	>21.3k[1]
4	<16.83[2]	4.82	<81.12	27.1k
5	12.45	4.22	52.59	32.8k
6	<15.20[2]	4.83	<73.41	30.6k
7	12.21	4.28	52.25	>12.4k[1]

[1] Illumination was not set high enough to exert the true VFW.
[2] Tests conducted at a high EMCCD temperature exhibit a spatial pattern (Figure 13) caused by the dark current that causes the overestimation of the k-gain and, as a result, of the RON.

Table 11: Power usage of the CPE during the TVAC campaign.

Plateau	Power (low)	Power (high)	Derived power at 1 FPS
1	11.8	14.0	12.06
2	12.2	14.5	12.47
3	11.8	13.7	12.02
4	12.3	14.6	12.57
5	11.8	13.7	12.02
6	12.5	14.9	12.78
7	11.8	13.7	12.03

cycling, it was discovered that the LED that was providing the illumination exhibited a much lower luminosity when it was cold. After the plateau #3, the light intensity was increased. On plateau #7, time constraints prevented the completion of the whole data acquisition, which restricted the maximum integration time that could be used.

5.1.4 Power consumption

The telemetry gathered during the TVAC campaign was used to analyze the power consumption of the CPE. The power consumption is measured using the CPE's own voltage and current monitoring capabilities. Both the voltage and the current of the first stage buck converter converter's output are measured, allowing one to infer the total power consumption of the CPE.

Figure 15 shows the power measured during the whole TVAC campaign. That figure shows that on average the power drawn by the CPE oscillates between two levels, which represent the exposing state (lower power) and the read-out state (higher power). Those two values drift as a function of the temperature since the static power of the CPE increases with temperature. In order to measure the power when operating at 1 FPS, the following formula is used:

$$P_{1fps} = P_{high} * 0.12 + P_{low} * (1 - 0.12),$$

where 0.12 represents the proportion of the time spent in read-out when running at 1 Frame per second (FPS).

The low and high levels for each of the plateaus are presented in Table 11, together with the derived power at 1 FPS. See Section 5.1.2 for a definition of each of the plateaus.

5.2 Vibrations campaign

The vibration campaign took place at CSA's DFL in May 2023. Vibration tests parameters were derived from NASA's qualification standards and were defined as Maximum Predicted Environment (MPE) + 3dB for 1 minute, each of 3 axes. The objective of these tests were to verify the vibration requirements of 6.8g Root mean square (RMS) for 1 minute/axis in the 20-2000 Hz range and to determine the CPE first mode of resonance for each axis. Tests were conducted in the order

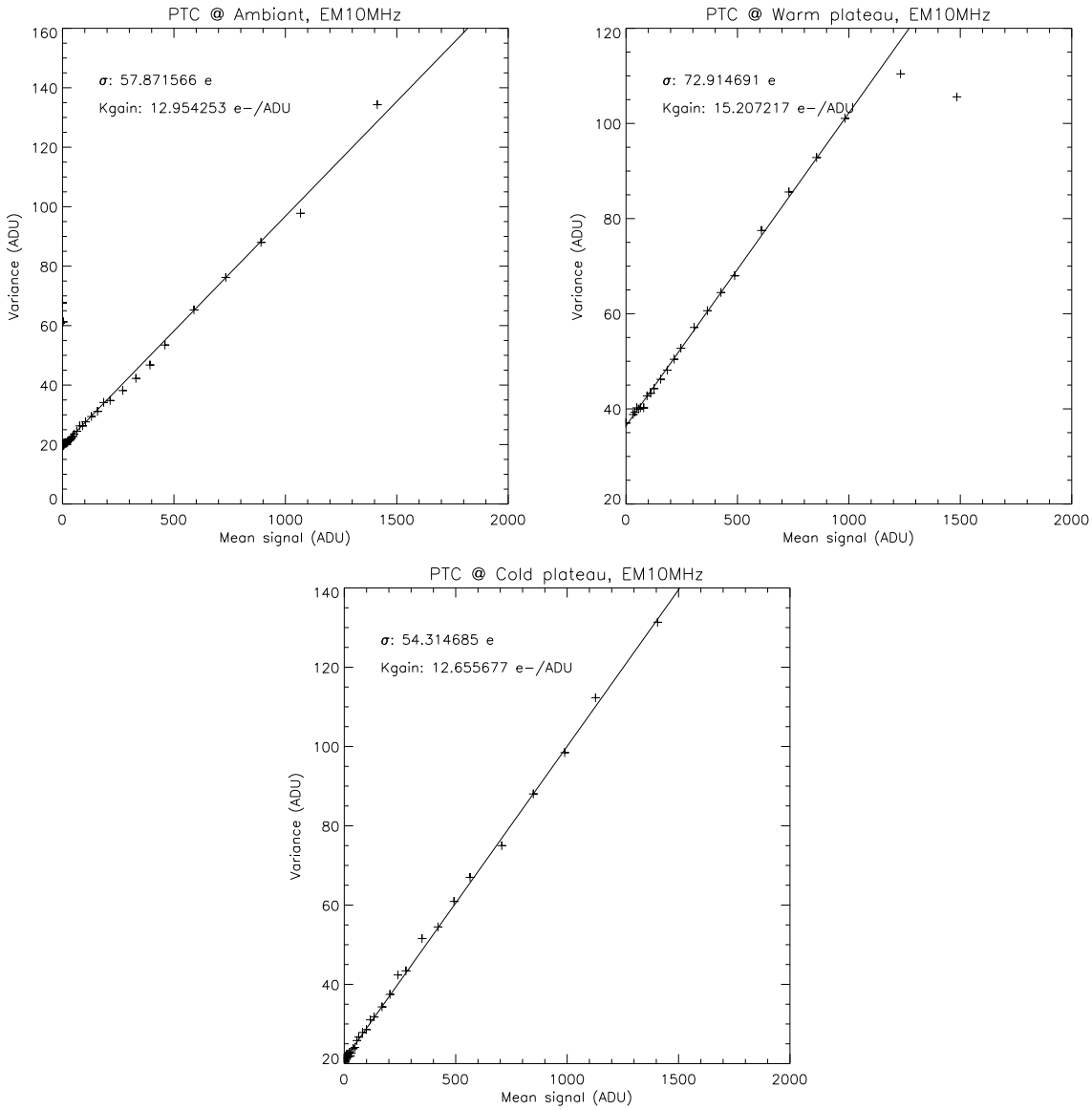

Figure 14: PTC results in TVAC for the DI mode. **Top left**: Ambiant temperature (Plateau #1). **Top right**: Warm plateau (Plateau #2). The variance at 0 signal is overestimated due to the high level of dark current which prevented acquiring a dark reference frame. **Bottom:** Cold plateau (Plateau #3).

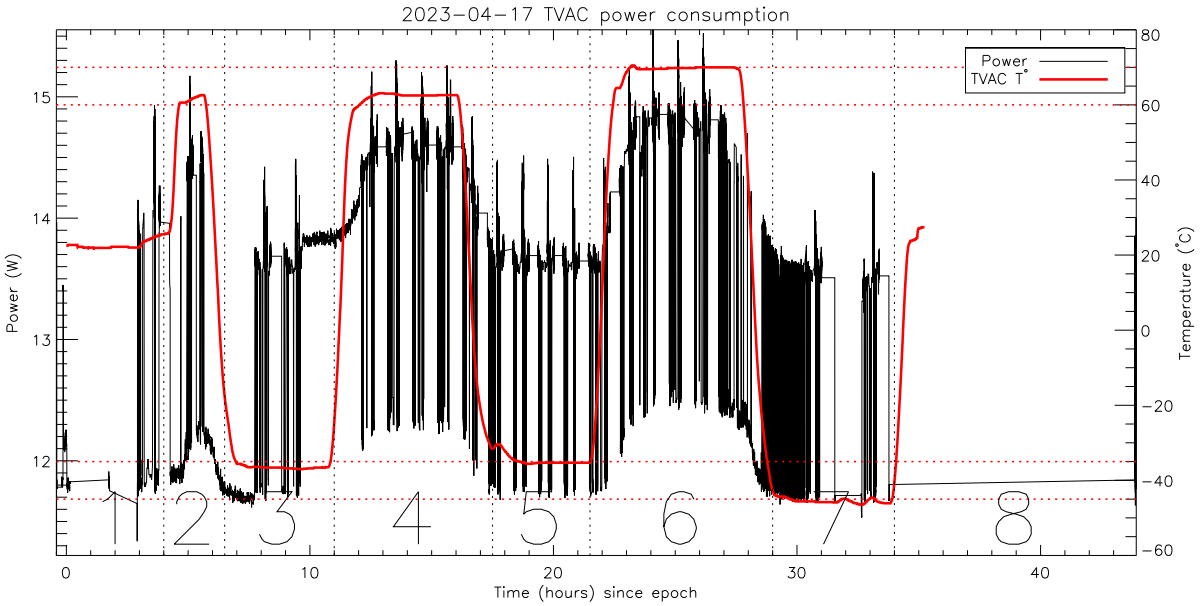

Figure 15: Power usage of the CPE during the TVAC campaign.

Table 12: Vibration tests sequence.

Axis	Description	Frequency range	Input level
1 x	Resonance survey	20–2000 Hz, 1 octave/minute	0.5 g
2 x	Random vibrations	20–2000 Hz, 1 min/axis	6.8 g RMS
3 x	Resonance survey	20–2000 Hz, 1 octave/minute	0.5 g
Visual inspection of the prototype and reduced functional tests			
4 z	Resonance survey	20–2000 Hz, 1 octave/minute	0.5 g
5 z	Random vibrations	20–2000 Hz, 1 min/axis	6.8 g RMS
6 z	Resonance survey	20–2000 Hz, 1 octave/minute	0.5 g
Visual inspection of the prototype and reduced functional tests			
7 y	Resonance survey	20–2000 Hz, 1 octave/minute	0.5 g
8 y	Random vibrations	20–2000 Hz, 1 min/axis	6.8 g RMS
9 y	Resonance survey	20–2000 Hz, 1 octave/minute	0.5 g
Visual inspection of the prototype and reduced functional tests			

defined in Table 12. For acceleration measurements, the acceleration sensors were installed on the prototype itself and on the shaker table for piloting the shaker, as shown in Figure 16.

The random vibration levels were defined based on NASA's minimum workmanship vibration levels for components below 50 kg[19] as detailed in Table 13 and Figure 17.

After the execution of the random vibration on each axis, reduced functional tests were ran. This involved acquiring a PTC to assess the stability of the CPE.

5.2.1 Test results

Figure 18 shows the results of the pre- and post-vibration resonance survey for the X axis. Figure 19 shows the results of the reduced functional test ran after the X axis vibrations campaign. Similar data were gathered for the Z and Y axis as well. The results of the vibration campaign are summarized in Tables 14 and 15.

The first table provides the measured shift in frequency and amplitude of the first mode of resonance, before and after each axis. Since all of the axis show a shift in frequency of less than 5%, the tests results are considered successful.

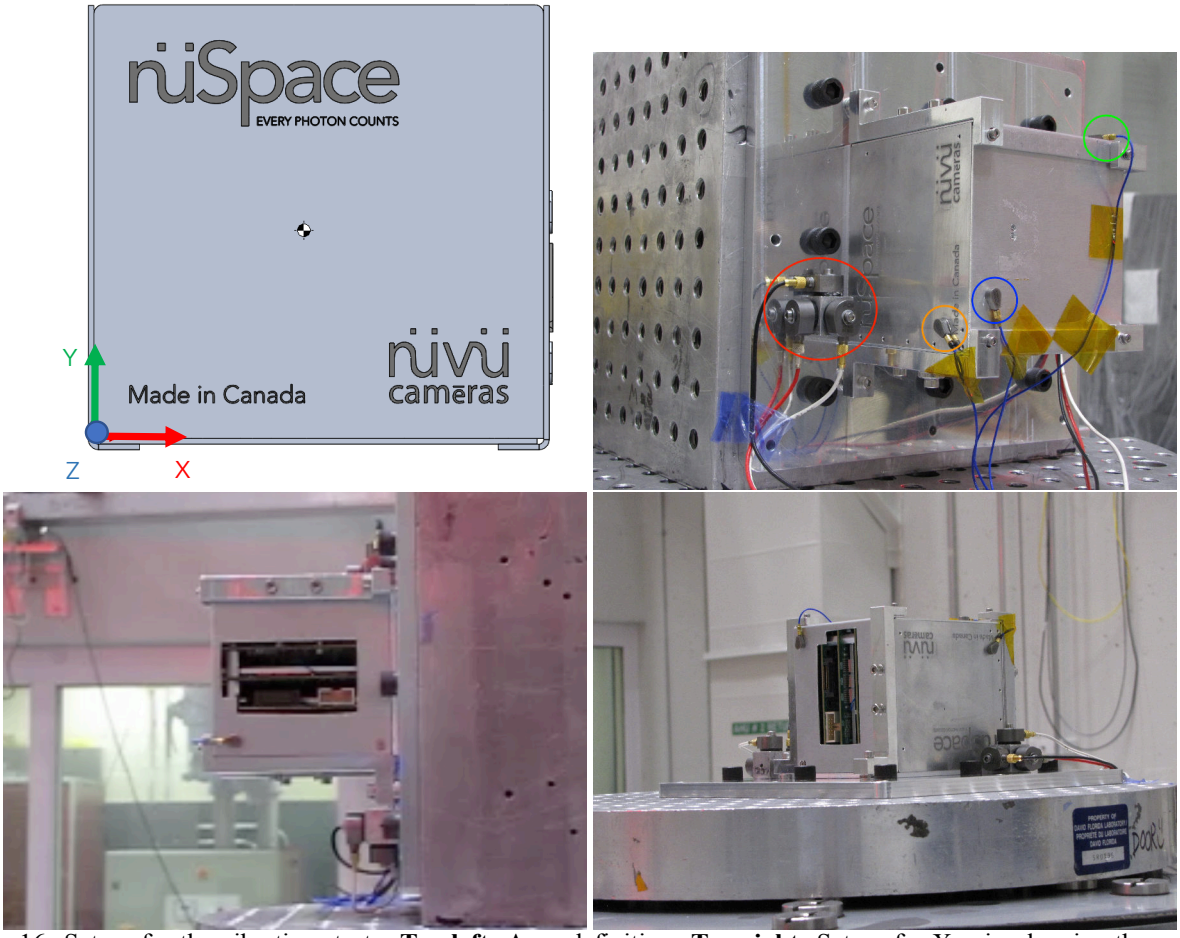

Figure 16: Set-up for the vibrations tests. **Top left**: Axes definition. **Top right**: Set-up for X axis, showing three of the six reference accelerometers (circled in red), and the measurement points for the X (green), Y (blue) and Z (orange) axes. **Bottom left**: Set-up for Z axis. **Bottom left**: Set-up for Y axis.

Table 13: Minimum Workmanship Random Vibration Test Level.

Frequency	Level
20 Hz	0.01 g^2/Hz
20 – 80 Hz	3 dB/oct
80 – 500 Hz	0.04 g^2/Hz
500 – 2000 Hz	-3 dB/oct
2000 Hz	0.01 g^2/Hz
Overall level	6.8 g RMS

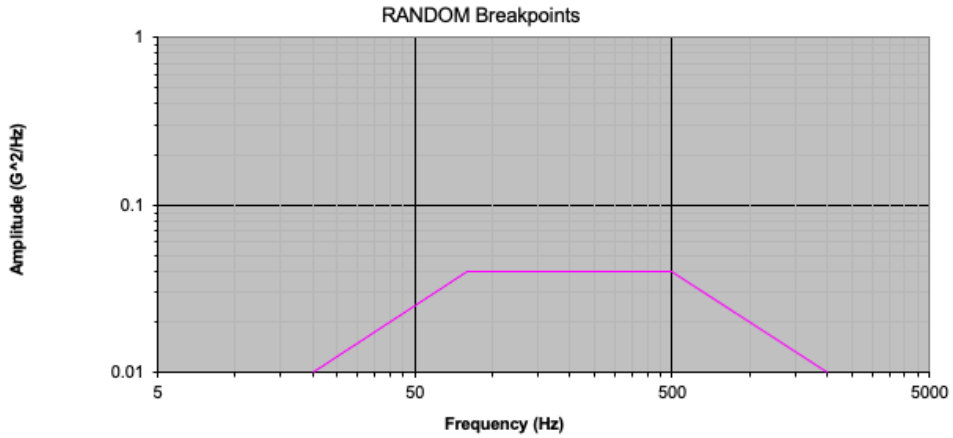

Figure 17: Acceleration Spectral Density (vs) Frequency

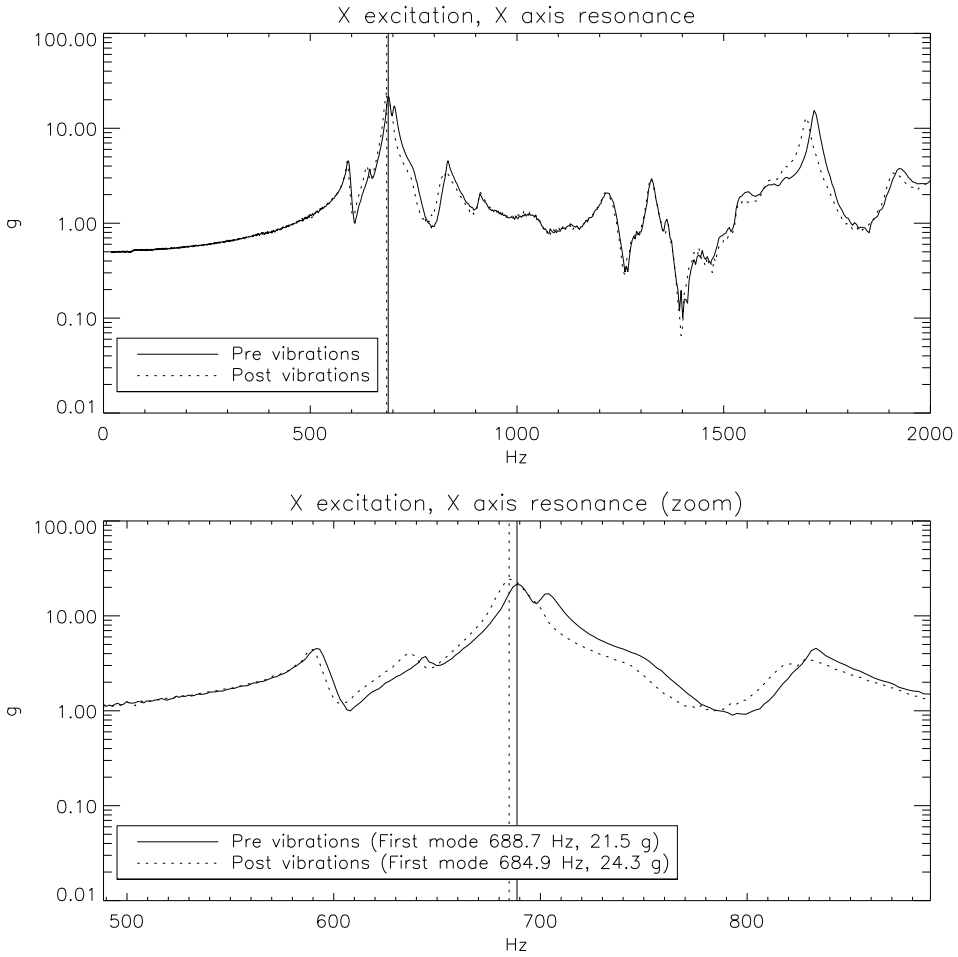

Figure 18: Example of the resonance survey, showing the results for the X axis. **Top**: Full width of the survey spectrum. **Bottom**: Zoom on the first mode.

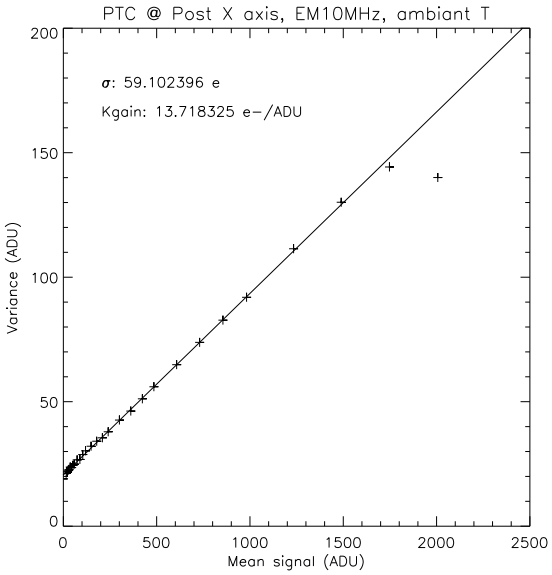

Figure 19: Post X-axis reduced functional test results.

Table 14: Results of the vibration test campaign.

Axis	Pre-vibes		Post-vibes		Delta	
	Frequency (Hz)	Amplitude (g)	Frequency (Hz)	Amplitude (g)	Frequency (%)	Amplitude (%)
X	688.7	21.5	684.9	24.3	-0.6	12.8
Z	577.0	7.2	569.1	5.8	-1.4	-19.2
Y	684.9	6.5	679.2	6.5	-0.8	0.9

Moreover, the overall shape of the spectrum did not change due to the random excitation, which is a healthy indication.[20] Referring to [21], the success criteria of a vibration test involves a shift of less than 20% in the amplitude of the first mode. Using this input, one can conclude that the shift in amplitude of 19.2% seen on the Z axis is within the acceptable range.

The next table summarizes the measured response and read-out noise during the individual reduced functional tests. No significant changes in the imaging performance were measured.

Figure 20 presents images that were acquired during the reduced functional tests. Those images represent the data acquired for the same integration time during each of the four reduced functional tests. Although the lightning conditions were not perfectly controlled since the prototype enclosure is not light tight, no significant changes in the image are observed. Figure 21 shows the difference between the pre-vibrations reduced functional test and the post-Y functional test. Except for a low frequency change in illumination that could be accounted for by the level of stray light entering the enclosure and the change in position of a speckle of dust on the EMCCD (towards the centre of the illuminated portion of the image), no change are observed. Together with the uniform results of the PTCs, this is an indication that the read-out electronics was

Table 15: Reduced functional test results during the vibration campaign.

Axis	k-gain (e^-/ADU)	RON (e^-)
Pre-vibrations	13.56	60.03
post-X	13.71	59.10
post-Z	13.86	59.74
post-Y	13.71	59.20

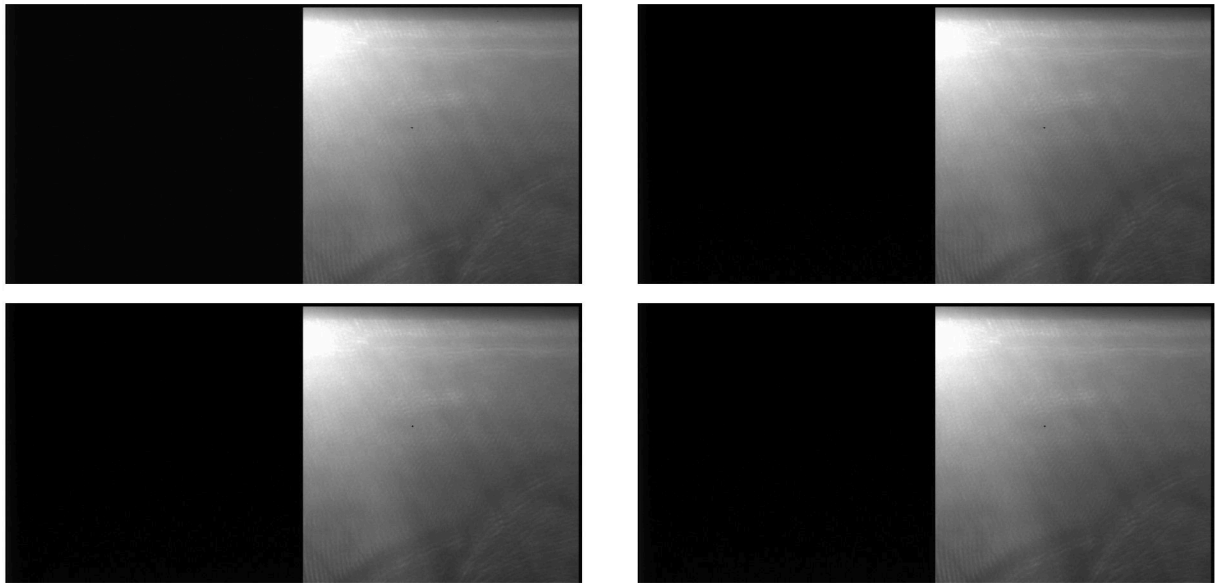

Figure 20: Example of comparable images taken with the prototype during the vibration campaign. **Top left**: Before the vibration campaign. **Top right**: Post X-axis. **Bottom left**: Post Z-axis. **Bottom right**: Post Y-axis.

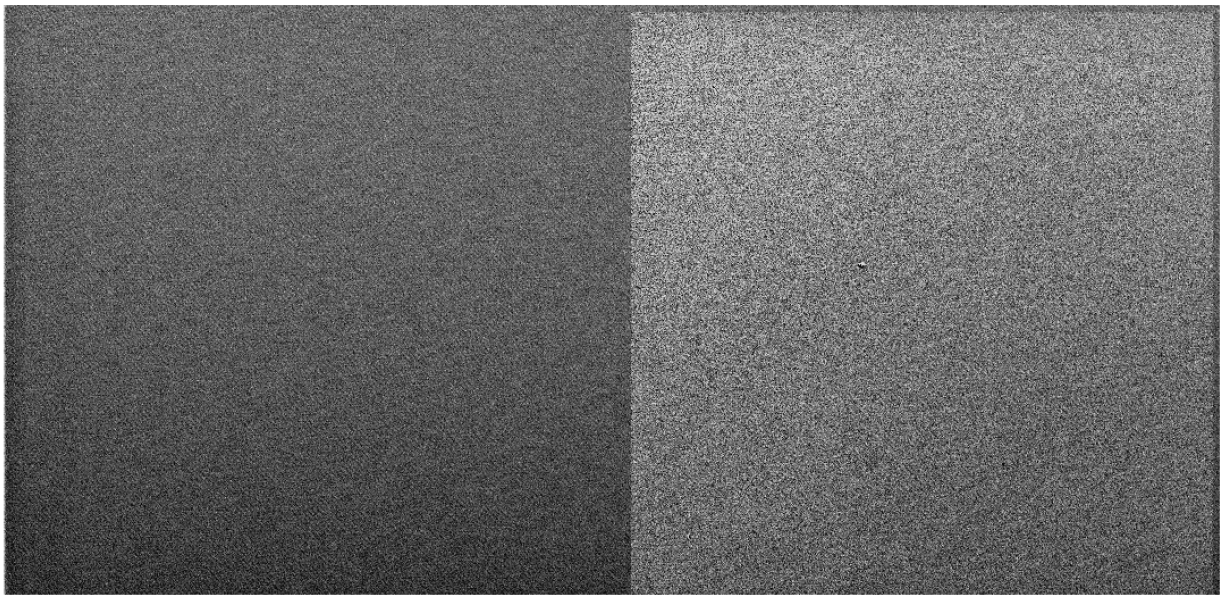

Figure 21: Differential image between the start and the end of the vibration campaign.

not affected by the vibrations.

6. CONCLUSIONS

This paper presented the design, characterization and qualification of a nüSpace camera. Its 1U footprint, low mass and low power consumption makes it well adapted to CubeSats. The imaging performance is without compromise compared to ground-based Electron Multiplying CCD (EMCCD) imaging solutions.

The test and qualification results presented show the nüSpace camera is well adapted for operating in a vacuum environment, over a wide range of temperature. While the thermal design was made with Low Earth Orbit (LEO) in mind,

the nüSpace camera can be adapted to other orbits, such as Geostationary Orbit (GEO) for meteorology applications, Sun Synchronous Orbit (SSO) for imaging & reconnaissance missions, as well as cis-lunar space for lunar reconnaissance and space debris identification missions.

Not limited to EMCCDs, the new space Camera Proximity Electronics (CPE) can also be used to drive conventional Charge Coupled Devices (CCDs). Its modular design and low noise makes the CPE of the nüSpace camera an architecture to build upon for custom requirements, such as for skipper or multi-channel CCDs.

By using the nüSpace platform as a stepping stone, Nüvü is also developing a solution for driving digital sensors such as CMOS in the space environment.

ACKNOWLEDGMENTS

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